IBIS ADVANCED TECHNOLOGY FOR SMALLSATS

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Abstract:

For many years, ESA has been involved in attempts to develop a commercially attractive radiation hardened true digital Sunsensor. Although both Galileo Avionica (IT) (now Leonardo) and TNO (NL) developed a sensor based on standard active pixel sensors (APS) none of these products became commercially successful. Although TNO started the development of a single chip true digital Sunsensor in 2004 and a prototype was successfully tested in 2011,[1] [2] the product was neither radiation hardened nor optimized for volume production. Development of this prototype into a real sensor was however never completed.

Although both a digital output and albedo sensitivity for a Sunsensor are two properties high on the Wishlist of many satellite builders, a single chip true digital Sunsensor has never been built before. This is why ESA started an ARTES program in cooperation with Lens R&D B.V. and Systematic Design B.V. that was supposed to lead to a cost-effective single chip radiation hardened true digital Sunsensor.

Advantages of such a sensor are:

- Minimum SWaP (Size, Weight and Power)
- True radiation hardened electronics due to the use of special design techniques and radiation hard cell designs
- High reliability due to the use of a minimum number of external components and re-use of an already proven mechanical concept
- High repeatability and yield due to the use of modern chip technology (0.18µm XFAB)

Combined with an optimization for volume manufacturing (as used by Lens R&D B.V. for the production of their BiSon and MAUS Sunsensors), the new IBIS sensor (Intensity Based Image sensor) is expected to provide the most cost-effective solution for high reliability Sun sensing available on the market once completed.

As the sensor will be facing the Sun directly in vacuum, a lot of emphasis is given to the reduction of the power consumption. Performance predictions as performed during the design of the chip showed an estimated power consumption of less than 130mW for the entire sensor. Initial measurements however show a power consumption of only 33mW which is significantly lower and a pleasant surprise.

Along with measurements that have shown the power consumption to be significantly lower than expected, the majority of the functionality could be proven on the first prototypes. A limited number of design errors will still need fixing before a fully functional sensor can be offered to the market. Next to this a significant amount of radiation testing will need to be done before the requested 15 years in GEO can be guaranteed. Despite a development trajectory of more than 20 Years, the sensor will however still be unique and provide a solution long sought for.

Precursor developments

The European Space Agency (ESA) initiated the developments of digital Sunsensors mid 1990's with both Galileo Avionica(IT) and TNO(NL). At that time the solutions were based on a radiation hardened CMOS imager an intensity reducing filter and a separate radiation hardened FPGA or ASIC for timing control and signal processing. Although these activities led to functional Sunsensors, they cannot be deemed a commercial success due to the high costs per sensor caused by the complexity of the solutions develop and consequential low market acceptance.

Whereas TNO never sold any of the sensors commercially and only flew a single flight qualification unit on the ESA PROBA-2 satellite, Galileo Avionica did sell a number of units commercially but sales was limited to some 20 units over a time span of 15 years. In the meantime this sensor has been taken out of production and is no longer available for sales.

Recognizing this issue and the need for a more commercially viable product, ESA initiated the development of a single chip digital Sunsensor while qualifying both the Galileo Avionica and TNO digital Sunsensors for flight with Galileo avionica. At that time the intention was to build satellites where all interfaces were digital and analogue signals were limited to temperature sensor signals as the maximum. Next to this albedo sensitivity was seen as an issue associated with analog Sunsensors and insensitivity to albedo a major improvement associated with digital Sunsensors.

Associated with the development of the Galileo constellation (European alternative to GPS) there was not only a timing restraint, but also a financial constraint and eventually the developed digital Sunsensors were discarded due to the high costs per sensor and replaced with an analogue Sunsensor with added baffle.

At about the same time the digital Sunsensors were rejected for use on Galileo, a Dutch Microsystems technology development program called MicroNed was initiated and TNO was awarded a contract to develop a fully autonomous true digital Sunsensor within the MISAT program (that was part of MicroNed).

Figure 1 Proposed TNO Digital Sunsensor revolution

Rationale for the development was an anticipated major reduction in budgets (size, weight, power and above all costs). Whereas the DSS was developed for the Galileo satellites and needed a 5V regulated power, the Proba-2 satellite demanded the use of unregulated 28V, thus adding significantly to the design on all before mentioned aspects. The idea of the so called µDSS was to be autonomously powered by means of a dedicated solar cell and to use an RF wireless communication link so as to save connectors and harness.

The program ended with a number of (significant) demonstrators only as shown in below Figure 2.

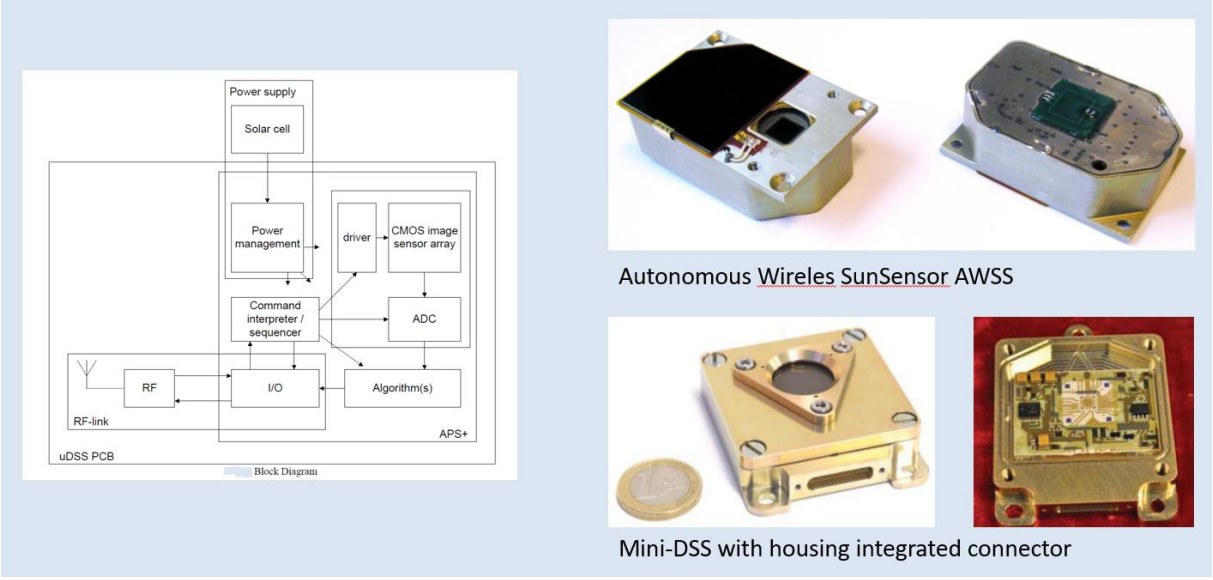

Figure 2 MicroNed MiSat program results

Two AWSS units have flown for many years on the Delfi-C3 nanosatellite build by the university of Delft and have shown (to our knowledge) operability of the first fully autonomous (none battery operated) sensors on board of a satellite.

Although some prototype Sunsensor were built and showed a very good accuracy [1] [2] the unit was never produced in volume nor actually flown in orbit.

Therefore, the program should mainly be seen as a precursor to the currently ongoing development of a significantly improved version.

De mini-DSS as the sensor without RF link was called has been a precursor unit to innovations regarding on chip functionality and design for assembly issues like housing integrated wirebondable connectors as currently used on the Lens R&D B.V. BiSon Sunsensors.

Requirements

Given the challenging nature of the developments, ESA formulated the requirements for the program in such a way that maximum flexibility was given to develop a commercially attractive product. The most relevant requirements being:

- accuracy over full field of view including albedo errors of less than 5°
- Calibrated accuracy over 30° field of view including albedo errors 1° (target 0.5°)
- Operating temperature range -40°C..+75°C (target -80°C..+100°C)
- 15 years in GEO
- Reliability <100FIT@30°C
- SEU tolerant
- <20k€/unit @6 units (target)

One of the main (deliberate) omissions in the requirements was the interface to be used. Some of the requirements that were challenged during contract negotiations and consequently discarded were:

- Hemispherical field of view
- 5V regulated or 12/28 or 50V unregulated.
- Internal redundancy

Requirements discussion.

The intention was to develop a very low power Sunsensor chip for the TNO µDSS, so as to be able to use a single solar cell for powering the circuit. This drove the initial design decisions which led to a row and column profiling approach [3]. In cause of this project however it became abundantly clear that not the actual solar cell sizing, but the overall power dissipation was the most important factor as thermal control for a small sensor system that is facing the Sun under vacuum conditions is a major challenge. As a result, from the beginning of the current project, the focus has been on reducing the power dissipation of the actual chip to the largest extend possible so as to optimize the changes of being able to manage the thermal control of the system. As a result, a 3.3V balanced SPI digital interface was chosen that is not commonly used on satellites, but is expected to fulfil the requirements of even the larger ESA missions.

The second and potentially most important parameter taken into consideration has been the total system cost in combination with the given reliability requirements. This combination of requirements mandates the use of as few as possible components, basically mandates the use of a single integrated circuit and prevents the use of a crystal oscillator. As a result, it was decided to go for a free running (asynchronous system) which is systematically under-sampled even at rates of 100Hz

Using the ESA developed Design Against Radiation Effects (DARE) libraries during the layout of the chip, expert help from ESA staff experienced in developing radiation hardened analogue circuits and preventing against latch up during the design and taking a number of generally know precautions, it is expected that the developed chip will be latch up free (LET >65MeV) Single Event Upset tolerant and total Ionizing dose resistant to well beyond 250krad (>1Mrad expected)

As the general mechanical construction will show a stark resemblance to the BiSon Analogue Sunsensors the same qualification program consisting of 40g sine, 34g random and 3000g pyro shock is foreseen and expected to be completed without any significant issues.

To improve the market potential the initial qualification is foreseen to span -40°C..+85°C as it is believed that a slightly higher operating temperature than required will ease accommodation on board of a satellite. It should be noted that due to the provided electronic baffling it is expected that the sensors will not be mounted on brackets anymore, thus easing thermal control through better coupling with the satellite structure.

Implementation.

After an extensive design period, the chip dubbed IPS+ was finally produced and functional testing has been performed.

The chip itself measures only 6.5mm*5.5mm and is realized in XFAB 0.18µm CMOS technology. In order to improve reliability and storage lifetime, the bond pads have been re-metalized with a palladium gold coating so as to avoid purple plague (in line with other high reliability optical sensors that are not hermetically sealed). In order to further improve the reliability of the overall system, the sensor has large bond pads that can accommodate a double wire bond for every connection.

The overall solution only requires three resistors and two capacitors in theory, but a testbed was created that had two additional capacitors added. Test without these capacitors still need to be performed. Figure 3 shows the actual test board layout used. On this picture the double wire bonds (produced by means of automated wire bonding) can be clearly seen as well as the bleed resistor R2 which serves no purpose but to avoid charging of the circuit with respect to the housing. R3//C2 is a RC filter on the 3.3V power line and R1 sets the reference for the circuit's comparators.

The entire circuit is so compact that it fits within the area available in the BiSon housing. This results in a solution that can use a large part of the available qualification and production tooling. (Thus, saving significant development costs.) It is the intention to start selling the testbeds as a Cubesat digital Sunsensor we dubbed µIBIS. Next to this, the development of the testbed (based on a standard 9 pin

nano-D connector) led to a third product for Lens R&D B.V. the radiation hardened cubesat Sunsensor MAUS as shown in Figure 4.

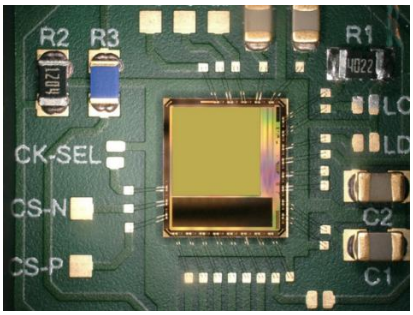

Figure 3 IPS+ testboard layout

Figure 4 Testbed, µIBIS and MAUS

Although of modest size, the complexity of the chip developed shouldn't be underestimated as shown in *Figure 5*

The circuit contains:

In the analogue part:

- Latching current limiter
- Undervoltage lockout
- 3 low dropout generators
- Power on reset circuit
- Reference source
- oscillator
- Temperature sensor with interface circuits and analogue to digital converter
- Analogue circuits test bus

In the pixel and readout part

- 384*384 pixel array
- Line and column drivers, readout circuits and comparators

In the configuration part

- Configuration registers
- Array drive and timing circuits
- Watch dog timer
- Digital test bus

In the sunspot detection and interface part

- Bright and dead pixel detection
- Sun spot size filtering
- Triple voting redundant centroid determination
- SPI interface
- Differential drivers

All in all, these subcircuits constitute a system on chip which is optimized to be both radiation hardened and cost effective, while in general expected to significantly exceed the set specifications.

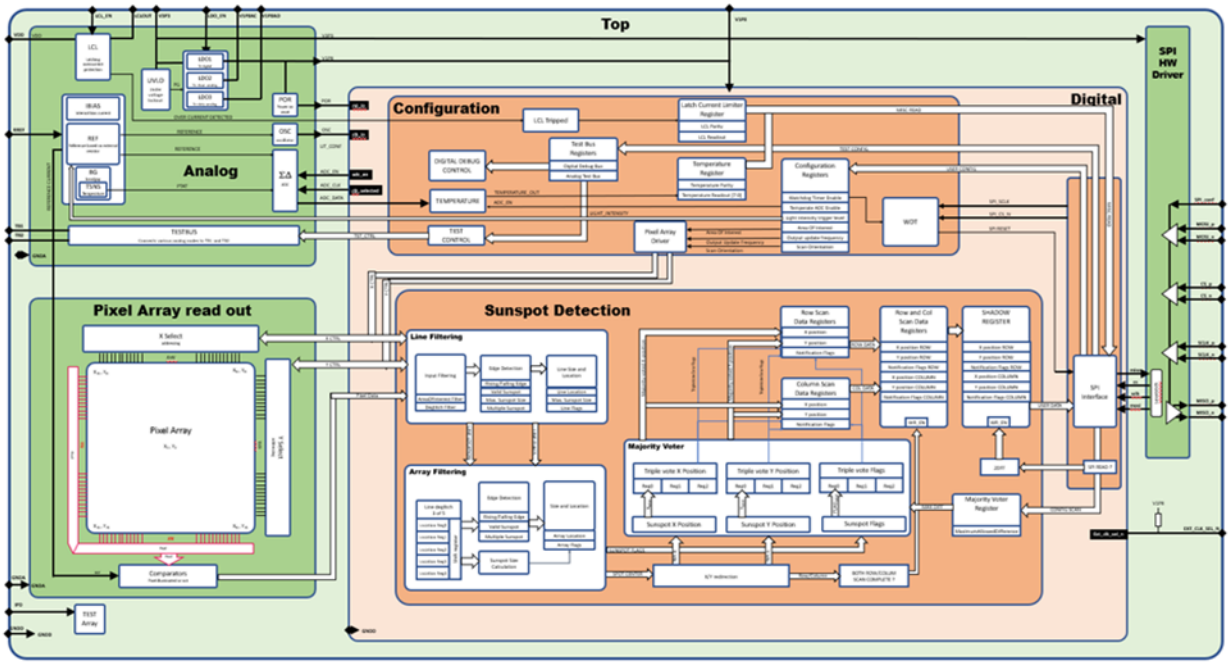

Figure 5 IPS+ functional diagram

Sole exception to this, is the radiation related lifetime requirement.

15 years in orbit after electric orbit raising leads to very harsh radiation requirements for a sensor that is mounted on the outside of the satellite. As typically no protection from cosmic radiation is provide by the satellite for one hemisphere, the packaging of the housing will need to be optimized to be able to cope with the high radiation environment based on the proven radiation resistance of the IPS+ chip.

This means, that the design of the housing can only be optimized after the radiation resistance of the chip has been proven to avoid adding an abundance of shielding.

As additional shielding will add costs to the sensor, the additional radiation resistance requirements posed to the sensor so it can operate for 15 years in GEO orbit after electric orbit raising is expected to lead to a more expensive solution. This in turn would lead to additional costs for all other applications and might not lead to an optimal solution.
The majority of sensors are expected to be sold for LEO applications as for these orbits albedo errors are more of an issue than for GEO orbits. Therefore, it is expected that a specific trade will be devoted to the question for which orbit the sensors should be optimized in the future and which radiation withstanding capabilities are required to cover the majority of turnover in the most cost-effective way.

Test results

Testbeds have been built and measured.

During the built, a number of crucial assembly steps have been tried:

- the processes to glue all components to the board instead of soldering
- replacing aluminum with gold bondpads and thick gold layer to prevent corrosion.
- automated redundant wirebonding

Whereas the gilding of the bondpads with a non-porous gold layer has been successfully demonstrated, glueing of the nano-D connector with silver loaded epoxy is still under improvement (but only needed for the µIBIS and potentially replaced by regular soldering. The automated wirebonding was performed successfully, but it turned out that the width of the bondpads should be increased to avoid overhang of the ball bonds.

As such the prototype assembly has provided some valuable insights into potential future improvements.

It turned out that it is quite cumbersome to test all functionality despite the presence of both an analogue and digital test bus on board of the chip. This is due to the small size of the overall setup and proximity of wire-bonds to probing locations. As a result, a number of testbeds were severed during testing and currently only one functional prototype out of 5 produced is still functional.

During testing one of the prototypes was found to be partially non-functional. This was deemed to be caused by an on-chip failure that would have been detected if a known good die (KGD) test would have been performed before assembly of the chip into the breadboard/prototype. As a result, it has been concluded that a KGD test is required for a commercially attractive yield during production of the actual devices. This will add to development and test costs, but will avoid scrapping components later on in the production process, leading to a much higher cost increase.

Despite the cumbersome testing, the majority of functionality could be proven.

In the analogue part everything has proven to be functional within simulated parameters with exception of the temperature sensor. It turns out a level translator between the 1.8V core digital circuit and the 3.3V ADC was omitted and the ADC cannot be selected. Even though a temperature sensor is not needed for the correct functioning of the sensor, an on-board temperature sensor is seen as beneficial especially during qualification testing.

Functionality of the pixel and readout part has been proven

The digital interface is performing as expected

The digital processing part is largely working as expected but a major error in the interfacing with the pixel array causes all lines but one to be selected instead of one line. This error causes the need for a new design run. Furthermore, an unexplained issue in the sequencer causes the sensor to work as expected in the normal mode, but the also foreseen reverse scan mode doesn’t seem to work as intended. Last but not least, the digital test bus didn’t allow to inject test vectors properly in all cases which made it difficult to fully test the digital part.

It should be noted that the functionality of the triple voting redundancy could not be established as there is no possibility foreseen to force an error in this part of the circuitry. Therefore, the functionality of this part has only been proven by simulation.
Despite this, a proper Sun detection and position determination could be established by setting the Sun exclusion zone to a size within the Sun size rejection limit.

The later might need some further explanation.

As mentioned, an error in the addressing of the pixel array causes all lines of the array but one to be selected instead of one line only. As a result, generating a light spot on the array and detecting that light spot doesn't currently work. There are however two features implemented on board that allowed to perform a check of the centroid detection anyway.

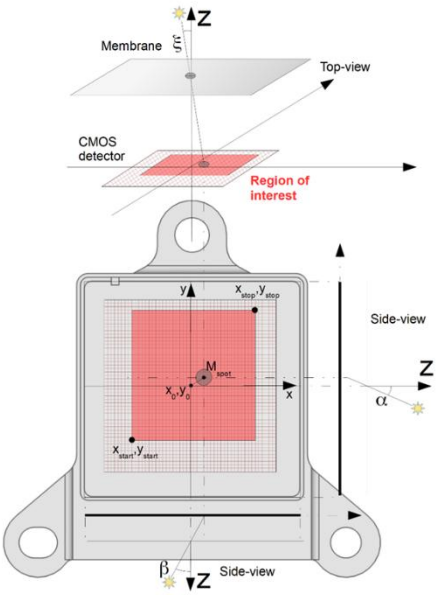

Figure 6 region of interest selection

A region of interest selection can be programmed that works much like an electronic baffle. In case a specular reflection can cause a false Sun detection within certain parts of the field of view, Sun presence evaluation of certain area's can be excluded by setting start/stop coordinates. This allows for selection of a rectangular area within the overall field of view for which there will be a Sun detection and exclusion of all areas outside this field of view. This feature was added because it was deemed to be adding to the flexibility of accommodation of the sensors. In addition, it will allow to use the sensors as an anomaly detector for protection of sensitive instrument from Sun illumination. (shuttering the instrument as soon as the Sun enters the set field of view and causes an alarm)

A second feature implemented is dead pixel filtering that is caused by the line filtering implemented to avoid falls Sun detection and reduce the effect of dead pixels on the centroiding.

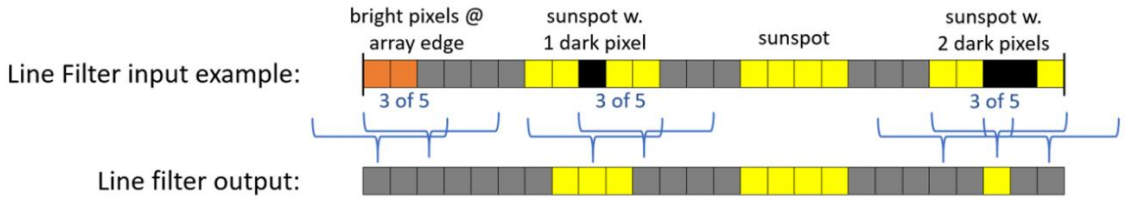

Figure 7 line filtering

As shown in above Figure 7, a sunspot with one dead or dark pixel will result in a sunspot that is at the right location.

Above two features allow to set the Sun evaluation area to an area the size of the expected sunspot. The line filtering then removes the one line that is not selected as if it is a dead pixel and the sensor will determine the centroid of the spot when the pixels are illuminated as if there is a Sun detected. Using this trick, it could be established that the centroiding algorithm correctly determines the position of the sunspot and the centroiding algorithm performs as expected.

Future activities.

In order to fix the issues identified an updated chip design will be needed. This means that new simulation will have to be run new masks will have to be produced, new chips will have to be produced gilded and diced. In the meantime, the storage lifetime of the PCB's will be expired so new PCB's will need to be ordered with the special coating that will allow to perform the wire-bonding. Next to this, new housings will have to be produced and assembled once all components are procured.

This time the diced chips should be properly packaged so as to allow for KGD testing and long-term storage as well as automated assembly all while avoiding contamination to the largest extend possible. The KGD test will have to be developed and performed and assembly of new prototypes will need to be done before a re-test can be initiated.

In order to save some time on the development program, it may be decided to assemble a limited number of units with non-tested devices, but this subject is still under discussion.

First priority is to correctly conclude the current development program with an extensive report showing results and shortcoming before attempting to enter another phase of the development trying to fix all known issue and trying to avoid additional issues. No new chips are to be expected before Q2/2026 but we still hope to have some units for sale for cubesat applications by Q4/2026

Acknowledgement.

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References:

1. de Boom, C.W. et all, *ESA GNC.* **2011**, *Mini-DSS: MINIATURIZED HIGH-PRECISION SUN-ANGLE MEASUREMENT;* 2. *de Boer, B.M.. et all, ESA ICSO 2012, MiniDSS: a low-power and high-precision miniaturized digital Sun sensor*
2. *de Boer, B.M. et all, ESA ICSO 2012, MiniDSS: a low-power and high-precision miniaturized digital sun by sensor*
3. *Xie, N et all, ESA ICSO 2010, The APS+ : an Intelligent Active Pixel Sensor Centered on Low Power*